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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,123	02/07/2001	Anantha R. Sethuraman	5298-02501	9269

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	PAPER NUMBER
2823	9

DATE MAILED: 12/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,123	SETHURAMAN ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *08 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The objection to drawings, to claims 2-8, 10-16, 18-20 and 112-second-paragraph rejection to claims 1, 2, 3, 7, 10, 11, 15 and 17 are withdrawn in response to applicants' amendment filed 10/8/02.

2. Claims 1-22 are pending in the application.

3. Corrected drawings submitted on 10/8/02 are approved by the examiner.

Grounds of Rejection

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaso et al. (US 6,093,631) in view of applicants' admitted prior art (AAPA), including pages 1-6 and Figs. 1-4.

With respect claims 1, 3, 9, 11, 17, 21 and 22, Jaso et al. teach a method, comprising:

- etching a plurality of laterally spaced dummy trenches 20 into a dielectric layer 14 between a first trench 15d and a series of second trenches 15a/15b/15c (Fig. 11B);
- filling the dummy trenches 20 and the first 15d and the series of second trenches 15a/15b/15c with a conductive material 16 (Fig. 11C); and

- polishing the conductive material 16 to form dummy conductors in the dummy trenches 20 and interconnect in the first trench 15d and the series of second trenches 15a/15b/15c, wherein the dummy conductor are electrically separate from the plurality of electrically conductive features and co-planar with the interconnect.

Jaso et al. do not teach that the first trench is a relatively wide trench and the series of second trenches are relatively narrow trenches. AAPA, however, in an analogous art teaches forming a relatively wide trench 24, a series of relatively narrow trenches 22 (Fig. 2); filling the relatively wide trench 24 and the series of relatively narrow trenches 22 with a conductive material 28 (Fig. 3); polishing the conductive material 16 to form conductors in the series of relatively narrow trenches 22 and interconnect in the relatively wide trench 24, wherein a common dishing problem occurs at the upper surfaces of the conductors and the interconnect due to the presence of a dense material (dielectric layer 20) between the conductors and the interconnect.

Therefore, at the time of the invention was made, one artisan in the art would have been motivated to apply the method of Jaso et al. to solve the dishing problem as demonstrated by AAPA, wherein the relatively wide trench 24 of AAPA can be treated as the first trench 15d of Jaso et al. and relatively narrow trenches 22 can be treated as the second trenches 15a/15b/15c of Jaso et al. The motivation/suggestions by doing so would be to apply the method of Jaso et al. to solve the dishing problem after polishing the conductors (narrow ones), the interconnect (wide one) and the dielectric layer existing between the conductors and the interconnect as shown in AAPA, i.e. to make the upper surfaces of conductors, the interconnect and the dielectric layer to be substantially coplanar as shown in Fig. 11D of Jaso et al.

Regarding claims 2, 10, 19 and 20, Jaso et al. teach that the conductive material comprises a metal , which can be a conventional metal such as Al, W, Ta or Ti, as evidenced by AAPA (page 3, lines 24-25).

Regarding claims 4, 12 and 18, the combination of Jaso et al. and AAPA teaches the polishing resulting in dummy dielectric protrusions between adjacent pairs of the dummy trenches, the dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of the dummy conductors.

Regarding claims 5-8, 13-16, Jaso et al. teach that the polishing comprises applying a polishing solution; applying an abrasive polishing surface to upper surface of the conductive material while moving the abrasive polishing surface relative to the upper surface, wherein the abrasive polishing surface comprises particles partially fixed into a polymer-based matrix and the particles comprises aluminum oxide or silicon dioxide (col. 1, lines 37-61).

Response to Arguments

6. Applicant's arguments filed 10/8/02 have been fully considered but they are not persuasive because of the reasons as follow.

Applicant' argument is on the ground that Figs.1-4 and related text ("AAPA") described in the present application is not prior art; and there is no desirability for modifying Jaso teachings with AAPA.

Applicant argues that neither applicant nor applicant's representative has ever stated or admitted that pages 1-6 and Figs.1-4 of applicant's disclosure are prior art. (second paragraph) This argument is not convincing.

In response to the denial of the prior art, the description of the drawings expressly states " Fig.2 depicts a partial cross-sectional view of a **conventional** semiconductor topography ...." (**page 10**); and " Fig. 4 depicts a partial cross-sectional view ..... using a **conventional** CMP technique, thereby forming a topological surface having elevational disparities;" (**page 10**); and " in FIG.1, a **typical** chemical-mechanical polishing (**page 2, line 11**). Accordingly, it would have been obvious to one of the ordinary skill in the art to appreciate that the conventional and typical techniques taught in Figs. 1-4 and related text are the **common knowledge** generally available to one of ordinary skill in the art **before** the filing date of the present application, i.e. prior art.

Applicant further argues that Jaso does not teach or suggest the desirability of, or provide motivation for including the dummy circuit design of Jaso in the semiconductor topography illustrated in Figs. 2-4 of application's disclosure. (third paragraph, page 6)

Contrary to the argument, Jaso **does** suggest the motivation to modify the teachings to apply in the situation demonstrated in Figs. 2-4 of application's disclosure. In particular, Jaso suggest that " in another aspect of the invention, a method is provided to set a predetermined high pattern factor designed limit of say 60-90%, preferably 70-80%. Using this method, the difference between the high pattern factor areas and the low pattern factor areas is minimized." (see **col. 3, lines 38-42**) Jaso further suggest that using a dummy circuit pattern layout in the invention would minimize the difference circuit density over the chip and wafer surface and provide a uniform metal surface after CMP. (col.3, lines 61-64). In other words, Jaso **inherently teaches or suggests** that by using the invention the dishing effect as shown in AAPA can be minimized between "a relatively narrow trenches", which is corresponding to the " low pattern

factor areas" and " a relatively wide trenches", which is corresponding to the " high pattern factor areas.' The pattern factor, according to Jaso, is defined by the area covered by the metal (i.e. conductive material) divided by the total area of the particular area or region. (col.3, lines 3-13) That is to say that Jaso's method would minimize the pattern factor difference as stated above but the difference **does** exist.

Therefore, at the time of the invention was made, one of the ordinary skill in the art would have been motivated to apply the method of Jaso et al. to solve the dishing problem as demonstrated by AAPA by including the dummy circuit design of Jaso in the semiconductor topography illustrated in Figs. 2-4 of application's disclosure.

Therefore, the 103(a) rejection as set forth in the previous Office action in view of the amendment filed 10/8/02 is deemed proper.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee
December 28, 2002

George Fourson
Primary Examiner
2823